QF01/0408-4.0E	Course Plan for Bachelor program - Study Plan Development and Updating Procedures/ Computer Science Department

Study plan No.	**2021/2022**		**University Specialization**		**Computer Science**	
Course No.	**0112 131**		**Course name**		**Digital Logic Design**	
Credit Hours	**3 hours**		**Prerequisite Co-requisite**		Discrete Mathematics	
Course type	☐ **MANDATORY UNIVERSITY REQUIREMENT**	☐ **UNIVERSITY ELECTIVE REQUIREMENTS**	**FACULTY MANDATORY REQUIREMENT**	☑ **Support course family requirements**	☐ **Mandatory requirements**	☐ **Elective requirements**
Teaching style	☐ **Full online learning**		☑ **Blended learning**		**Traditional learning**	
Teaching model	☐ **2 Synchronous: 1asynchronous**		☑ **2 face to face : 1synchronous**		**3 Traditional**	

Faculty member and study divisions' information (to be filled in each semester by the subject instructor)

Name	Academic rank	Office No.	Phone No.	E-mail	
Dr. Maher Nabelsi	**Associate professor**	**9332**	**-**	**nabulsi@zuj.edu.jo**	
Division number	**Time**	**Place**	**Number of students**	**Teaching style**	**Approved model**
				Blended	**2:1**

Brief description

Digital logic design is concerned with computer organization, architecture, operating systems, networks, and many other materials. This course introduces the following topics: **Digital systems, Number systems and conversions, Unsigned and signed binary numbers, Binary codes, Boolean Algebra and logic gates, The map method, Combinational circuits, MSI circuits, Sequential circuits, Registers and counters.**

Learning resources

Course book information (Title, author, date of issue, publisher ... etc)	Morris.M.Mano," **Digital Logic and Computer Design ",** 1st ed., Pearson, 2016.			
Supportive learning resources (Books, databases, periodicals, software, applications, others)	1. Morris.M.Mano, Michael Ciletti," **Digital design",** 5th ed., Prentice-hall , 2013 . 2. David Harris and Sarah Harris, "**Digital design and computer architecture ",** 2nd ed, Morgan Kaufmann, 2012. 3. David L. Prowse, "**Computer Structure and Logic** ",Pearson Education, 2011. 4. Charles , Larry Kinny, **"Fundamentals of Logic Design ",**6th ed. Thomson, 2009.			
Supporting websites	https://elearning.zuj.edu.jo			
The physical environment for teaching	☑ Class room	☐ labs	☐ Virtual educational platform	☐ Others
Necessary equipment and software	----------			
Supporting people with	----------			

special needs	
For technical support	----------

Course learning outcomes (S= *Skills, C= Competences K= Knowledge,)*

No.	Course learning outcomes	The associated program learning output code
	Knowledge	
K1	Providing the students with the required knowledge about the basic hardware components and digital systems of computer.	**MK3**
K2	Providing knowledge of binary codes and the unsigned and signed binary numbers.	**MK3**
K3	Developing the students' knowledge about Boolean algebra, logic gates, and the map method.	**MK3**
K4	Providing the students with the required knowledge about the combinational and sequential circuits.	**MK3**
	Skills	
S1	The student should understand the number systems and conversions.	**MS5**
S2	Represent the unsigned and signed numbers in binary system. Construct different binary codes.	**MS5**
S3	Apply Boolean algebra to describe digital circuits. Use the map method for simplification Boolean functions. Understand NAND & NOR implementations. Use don't care conditions in the map method.	**MS5**
S4	Define the combinational and sequential circuits. Design the combinational circuits (adder, subtractor, ...). Design MSI circuits (decoder, encoder, MUX, …).	**MS5**
	Competences	
C1	The ability to understand the number systems and conversions.	**MC2**
C2	The ability to construct different binary codes.	**MC2**
C3	The ability to construct simple digital circuits.	**MC2**
C4	The ability to differentiate between combinational and sequential circuits.	**MC2**

Mechanisms for direct evaluation of learning outcomes

Type of assessment / learning style	Fully electronic learning	Blended learning	Traditional Learning (Theory Learning)	Traditional Learning (Practical Learning)
First exam	0	**0**	-	0
Second / midterm exam	%30	%30	**%30**	30%
Participation / practical applications	0	0	**%20**	30%
Asynchronous interactive activities	%30	%20	**0**	0
final exam	%40	%50	**%50**	40%

Note: Asynchronous interactive activities are activities, tasks, projects, assignments, research, studies, projects, and work within student groups ... etc, which the student carries out on his own, through the virtual platform without a direct encounter with the subject teacher.

Schedule of simultaneous / face-to-face encounters and their topics

Week	Subject	learning style*	Reference **
1	**Digital systems.** **Number systems.** Conversions between systems.	Lectures	1-14
2	Complements. **Unsigned numbers.** **Signed numbers.**	Lectures	
3	**Binary codes.** Codes for decimal digits Parity code and error detection.	Lectures	14- 31
4	ASCII code. **Boolean Algebra and logic gates.** Theorems and properties.	Lectures	31-65
5	Boolean functions. Canonical and Standard forms, non-standard form. Logic operations and gates.	Lectures	
6	Buffer, inverter , AND, OR . NAND, NOR , E – OR , E -NOR .	Lectures	
7	**The map method.** Two, three and four- variable functions. Product of sums simplification. **Midterm exam.**	Lectures	65-103
8	NAND & NOR implementations. Don't care conditions. **Combinational circuits.**	Lectures	103-137
9	Design procedure. Half adder, full adder. Half sub-tractor, full sub-tractor. Analysis procedure.	Lectures	
10	Code conversion. Parity generator and parity checker. **MSI circuits.**	Lectures	137- 179
11	Parallel adder- subtractor circuit. Decoder, encoder. MUX, De-MUX.	Lectures	
12	**Sequential circuits.**	Lectures	179- 229

	Analysis of clocked sequential circuits.		
13	Flip-flops : SR , D JK , and T Excitation tables.	Lectures	
14	**Registers and counters.** Design of registers. Design of counters.	Lectures	229 - 247
15	General problems and applications. Review of previous chapters.	Lectures	
16	**Final Exam**		

*** Learning styles: Lecture, flipped learning, learning through projects, learning through problem solving, participatory learning ... etc.**
**** Reference: Pages in a book, database, recorded lecture, content on the e-learning platform, video, website ... etc.**

Schedule of asynchronous interactive activities (in the case of e-learning and blended learning)

Week	Task / activity	Reference	Expected results
1	Conversions between number systems.	https://elearning.zuj.edu.jo	Understanding
2	Represent unsigned and signed numbers in binary system.	https://elearning.zuj.edu.jo	Understanding
3	Addition and subtraction for unsigned and signed binary numbers.	https://elearning.zuj.edu.jo	Understanding
4	Construct binary codes.	https://elearning.zuj.edu.jo	Understanding and developing
5	Simplification of Boolean functions using logical identities.	https://elearning.zuj.edu.jo	Understanding and developing
6	Implementation of Boolean functions with logic gates.	https://elearning.zuj.edu.jo	Understanding
7	Simplification of Boolean functions using the map method.	https://elearning.zuj.edu.jo	Understanding and developing
8	Implement Boolean functions with NAND and NOR gates.	https://elearning.zuj.edu.jo	Understanding
9	Using don't care conditions on the map.	https://elearning.zuj.edu.jo	Understanding
10	Design procedure of combinational circuits.	https://elearning.zuj.edu.jo	Understanding
11	Design procedure of SSI circuits.	https://elearning.zuj.edu.jo	Understanding and developing
12	Design procedure of MSI circuits.	https://elearning.zuj.edu.jo	Understanding and developing
13	Design procedure of registers.	https://elearning.zuj.edu.jo	Understanding
14	Design procedure of counters.	https://elearning.zuj.edu.jo	Understanding
15			
16			